



## Description

### JMT N-channel Enhancement Mode Power MOSFET

#### Features

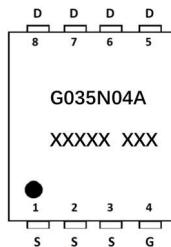
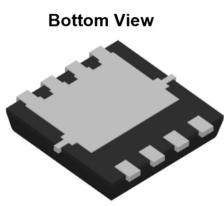
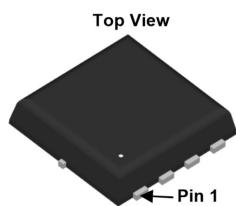
- 40V,100A
- $R_{DS(ON)} < 3.5\text{m}\Omega$  @  $V_{GS} = 10\text{V}$
- Lead free and Green Device Available
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead free product is acquired

#### Application

- Load Switch
- PWM Application
- Power management

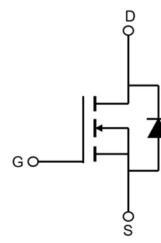


100% UIS TESTED!  
100%  $\Delta V_{ds}$  TESTED!



PDFN5X6-8L

Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
G035N04A	JMTG035N04A	TAPING	PDFN5X6-8L	13inch	2500	25000

## Absolute Maximum Ratings ( $T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
$V_{DSS}$	Drain-Source Voltage		40	V
$V_{GSS}$	Gate-Source Voltage		$\pm 25$	V
$I_D$	Continuous Drain Current		100	A
	$T_c = 100^\circ\text{C}$	65	A	
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>		400	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>		272	mJ
$P_D$	Power Dissipation	$T_c = 25^\circ\text{C}$	61	W
$R_{eJC}$	Thermal Resistance, Junction to Case		2	$^\circ\text{C}/\text{W}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

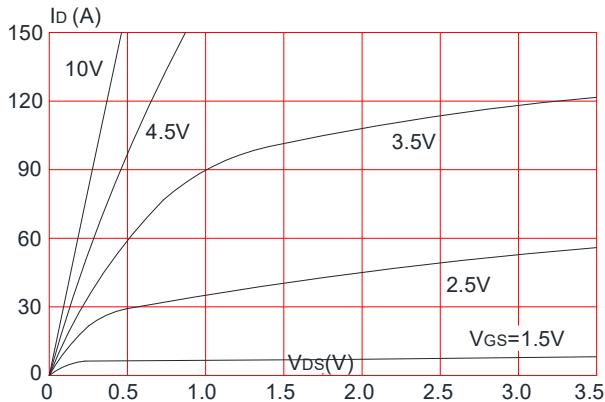
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$	40	-	-	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS}=40\text{V}$ , $V_{GS}=0\text{V}$ ,	-	-	1.0	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Body Leakage Current	$V_{DS}=0\text{V}$ , $V_{GS}= \pm 25\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2	2.8	4	V
$R_{DS(\text{on})}$	Static Drain-Source on-Resistance note3	$V_{GS}=10\text{V}$ , $I_D=30\text{A}$	-	2.7	3.5	$\text{m}\Omega$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=20\text{V}$ , $V_{GS}=0\text{V}$ , $f=1.0\text{MHz}$	-	4900	-	pF
$C_{oss}$	Output Capacitance		-	528	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	317	-	pF
$Q_g$	Total Gate Charge	$V_{DS}=20\text{V}$ , $I_D=30\text{A}$ , $V_{GS}=10\text{V}$	-	80	-	nC
$Q_{gs}$	Gate-Source Charge		-	17	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	21	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=20\text{V}$ , $I_D=30\text{A}$ , $R_L=1\Omega$ , $R_{\text{GEN}}=3\Omega$ , $V_{GS}=10\text{V}$	-	21	-	ns
$t_r$	Turn-on Rise Time		-	32	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	71	-	ns
$t_f$	Turn-off Fall Time		-	40	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	100	-	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	400	-	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$ , $I_S=30\text{A}$	-	-	1.2	V
$t_{rr}$	Body Diode Reverse Recovery Time	$T_J=25^\circ\text{C}$ , $I_F=30\text{A}, dI/dt=100\text{A}/\mu\text{s}$	-	27	-	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge		-	46	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

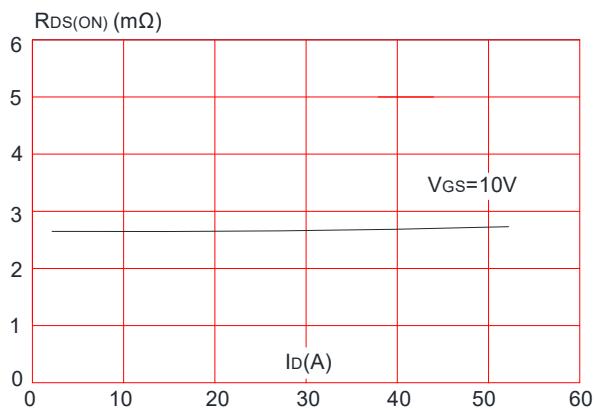
2. EAS condition:  $T_J=25^\circ\text{C}$ ,  $V_{DD}=20\text{V}$ ,  $V_G=10\text{V}$ ,  $R_G=25\Omega$ ,  $L=0.5\text{mH}$ ,  $I_{AS}=33\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$ , Duty Cycle $\leq 0.5\%$

## Typical Performance Characteristics

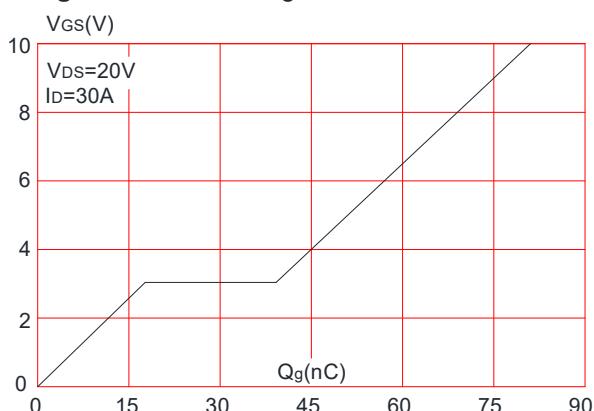
**Figure 1:** Output Characteristics



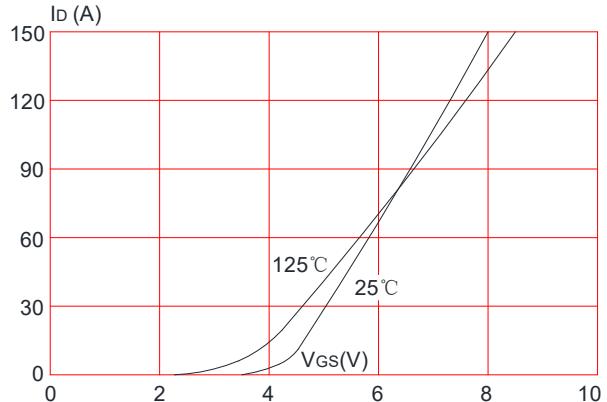
**Figure 3:** On-resistance vs. Drain Current



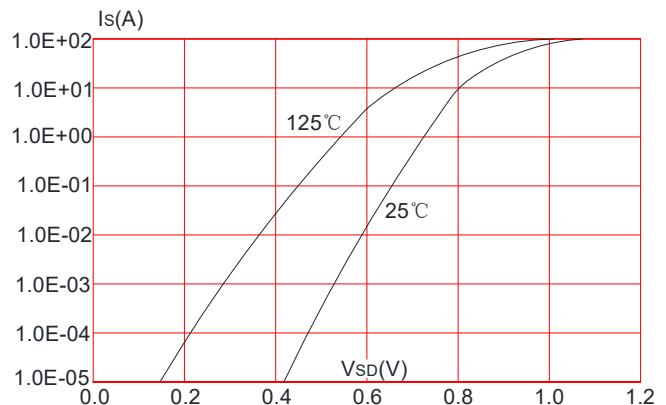
**Figure 5: Gate Charge Characteristics**



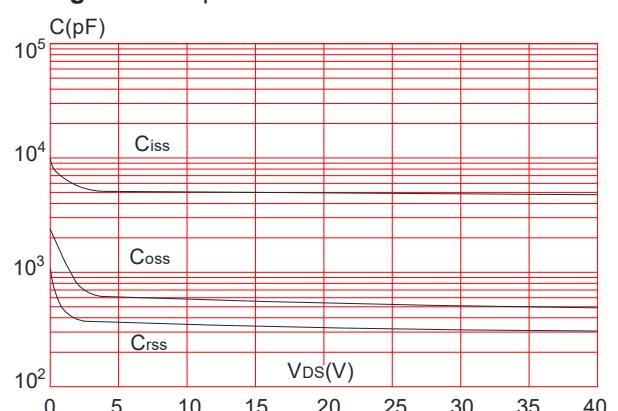
**Figure 2:** Typical Transfer Characteristics



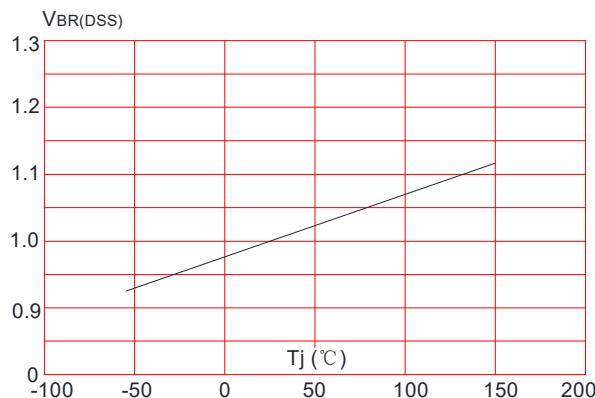
**Figure 4:** Body Diode Characteristics



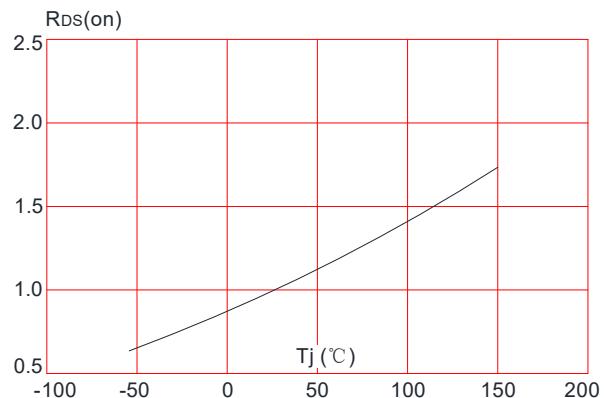
**Figure 6:** Capacitance Characteristics



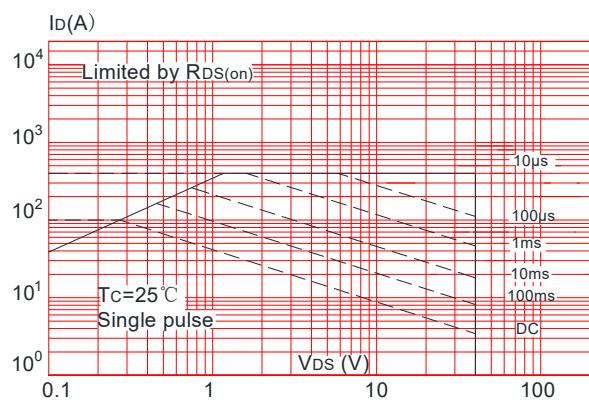
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



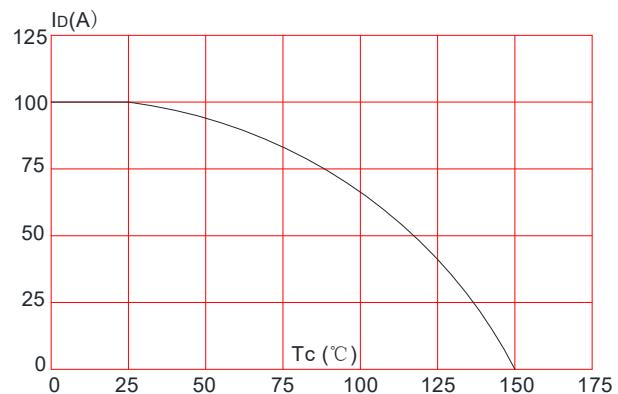
**Figure 8:** Normalized on Resistance vs. Junction Temperature



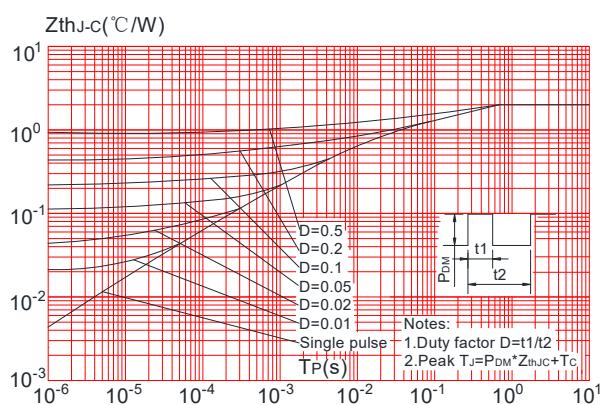
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure 11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



## Test Circuit

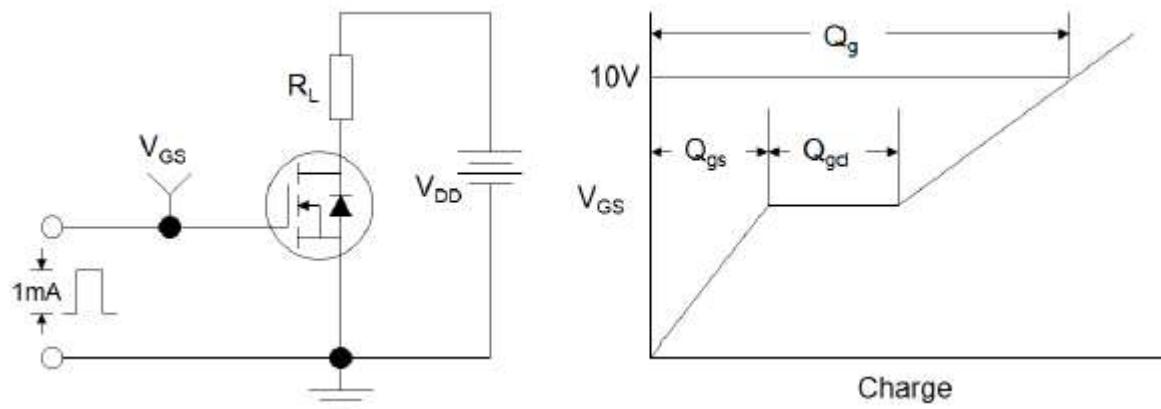


Figure1:Gate Charge Test Circuit & Waveform

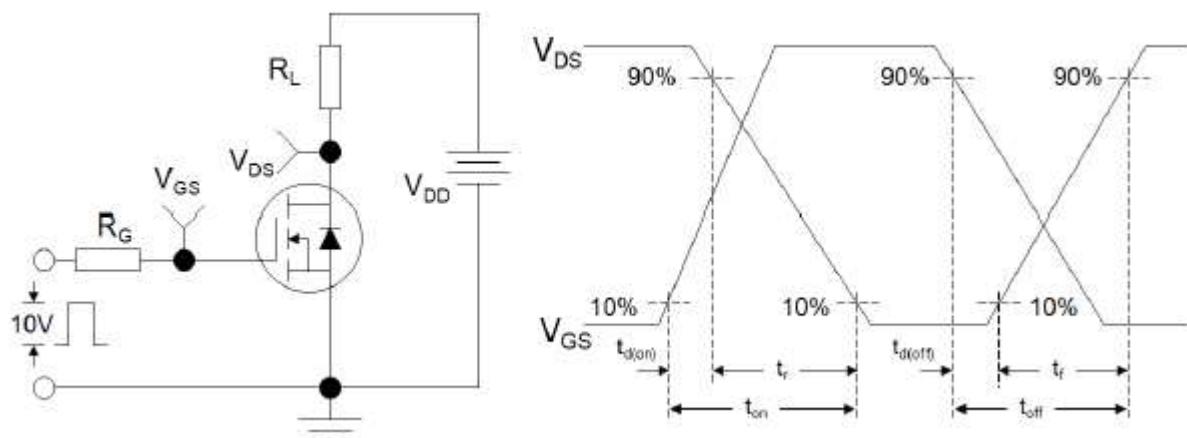


Figure 2: Resistive Switching Test Circuit & Waveforms

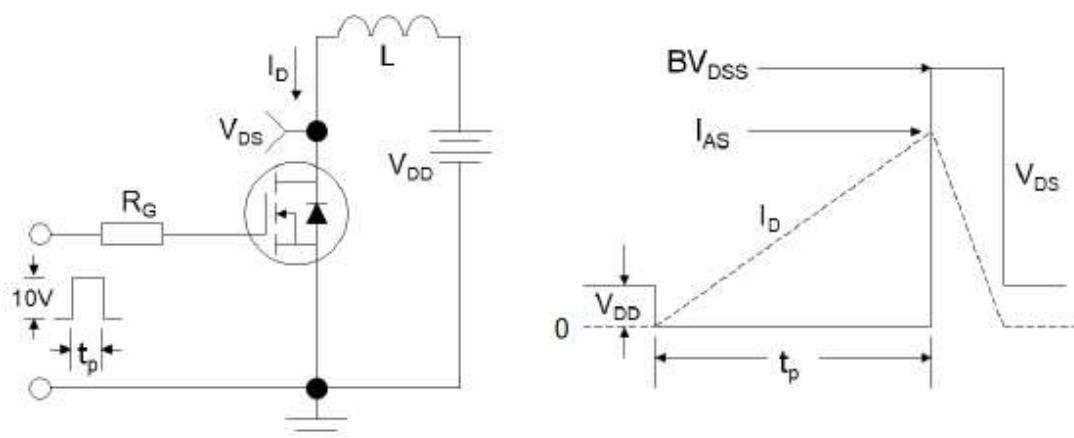
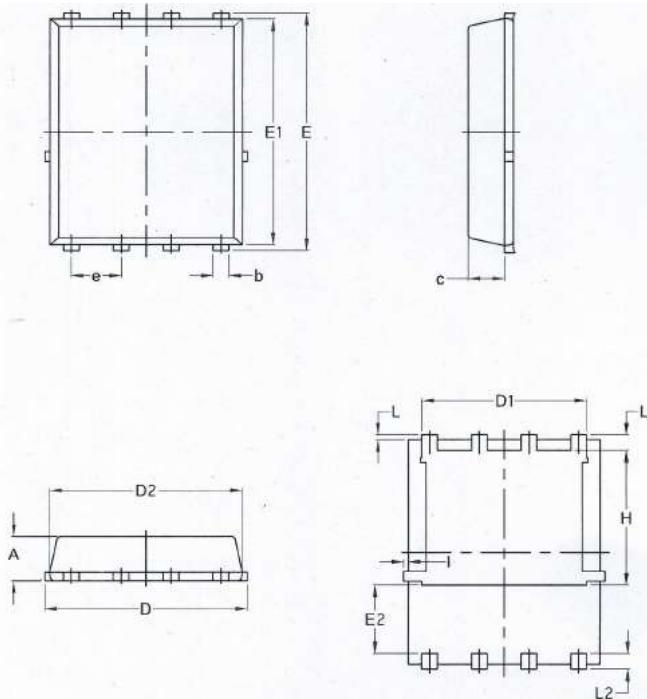


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



## Package Mechanical Data- PDFN5X6-8L



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	—	0.0630	—
e	1.27	BSC	0.05	BSC
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	—	0.18	—	0.0070

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